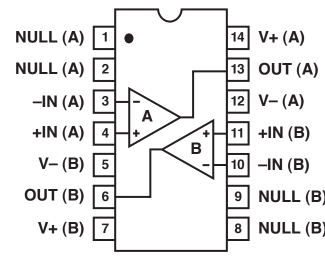
Dual, Low Noise, Low Offset Instrumentation Operational Amplifier

OP227

FEATURES

Excellent Individual Amplifier Parameters
Low V_{OS}, 80 μV Max
Offset Voltage Match, 80 μV Max
Offset Voltage Match vs. Temperature, 1 μV/°C Max
Stable V_{OS} vs. Time, 1 μV/M_O Max
Low Voltage Noise, 3.9 nV/$\sqrt{Hz}$ Max
Fast, 2.8 V/μs Typ
High Gain, 1.8 Million Typ
High Channel Separation, 154 dB Typ

PIN CONNECTIONS



NOTE
1. DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED; THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B
2. V–(A) AND V–(B) ARE INTERNALLY CONNECTED VIA SUBSTRATE RESISTANCE

GENERAL DESCRIPTION

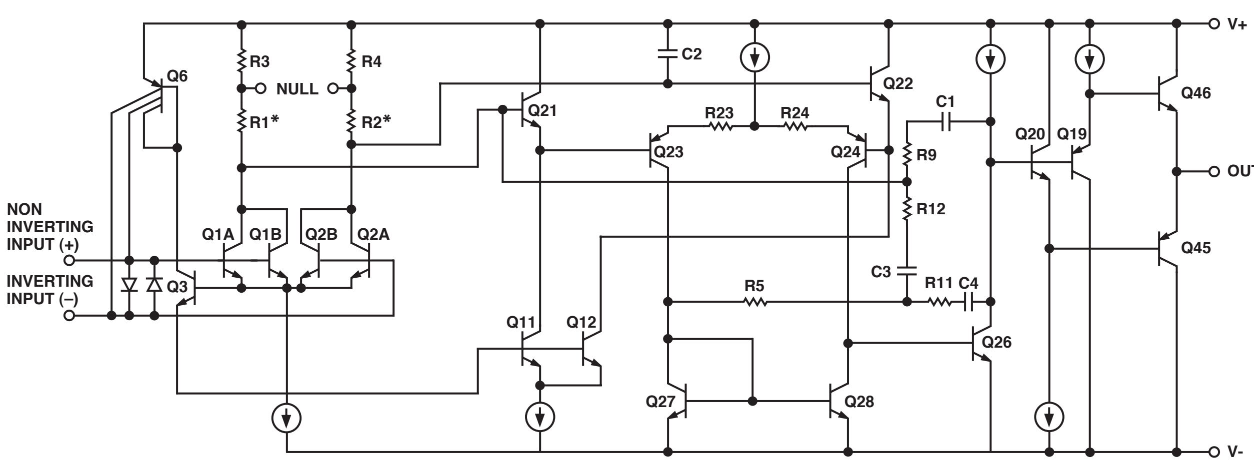
The OP227 is the first dual amplifier to offer a combination of low offset, low noise, high speed, and guaranteed amplifier matching characteristics in one device. The OP227, with a V_{OS} match of 25 μV typical, a TCV_{OS} match of 0.3 μV/°C typical and a 1/f corner of only 2.7 Hz is an excellent choice for precision low noise designs. These dc characteristics, coupled with a slew rate of 2.8 V/μs typical and a small-signal bandwidth of 8 MHz typical, allow the designer to achieve ac performance previously unattainable with op amp based instrumentation designs.

When used in a three op amp instrumentation configuration, the OP227 can achieve a CMRR in excess of 100 dB at 10 kHz. In addition, this device has an open-loop gain of 1.5 M typical with a 1 kΩ load. The OP227 also features an I_B of ±10 nA typical, an I_{OS} of 7 nA typical, and guaranteed matching of input currents between amplifiers. These outstanding input current specifications are realized through the use of a unique input current cancellation circuit which typically holds I_B and I_{OS} to ±20 nA and 15 nA respectively over the full military temperature range.

Other sources of input referred errors, such as PSRR and CMRR, are reduced by factors in excess of 120 dB for the individual amplifiers. DC stability is assured by a long-term drift application of 1.0 μV/month.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage versus temperature, noninverting bias current, CMRR, and power supply rejection ratio. This unique dual amplifier allows the elimination of external components for offset nulling and frequency compensation.

SIMPLIFIED SCHEMATIC



*R1 AND R2 ARE PREMATURELY ADJUSTED AT WAFER TEST FOR MINIMUM OFFSET VOLTAGE.

REV. A

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OP227–SPECIFICATIONS

Individual Amplifier Characteristics (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP227E Min	OP227E Typ	OP227E Max	OP227G Min	OP227G Typ	OP227G Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}	Note 1		20	80		60	180	µV
LONG-TERM V_{OS} STABILITY	V_{OS}/Time	Notes 2,4		0.2	1.0		0.4	2.0	µV/M_O
INPUT OFFSET CURRENT	I_{OS}			7	35		12	75	nA
INPUT BIAS CURRENT	I_B			±10	±40		±15	±80	nA
INPUT NOISE VOLTAGE	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz Notes 3,5		0.08	0.20		0.09	0.28	µV p-p
INPUT NOISE VOLTAGE DENSITY	e_n	f_O = 10 Hz[3] f_O = 30 Hz[3] f_O = 1000 Hz[3]		3.5 3.1 3.0	6.0 4.7 3.9		3.8 3.3 3.2	9.0 5.9 4.6	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
INPUT NOISE DENSITY	i_n	f_O = 10 Hz[3, 6] f_O = 30 Hz[3, 6] f_O = 1000 Hz[3, 6]		1.7 1.0 0.4	4.5 2.5 0.7		1.7 1.0 0.4	 0.7	$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
INPUT RESISTANCE Differential Mode Common Mode	 R_{IN} R_{INCM}	 Note 7	 1.3	 6 3		 0.7	 4 2		 MΩ GΩ
INPUT VOLTAGE RANGE	IVR		±11.0	±12.3		±11.0	±12.3		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±11 V	114	126		100	120		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4 V to ±18 V		1	10		2	20	µV/V
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	$R_L \geq$ 2 kΩ, V_O = ±10 V $R_L \geq$ 600 kΩ, V_O = ±10 V	1000 800	1800 1500		700 600	1500 1500		V/mV V/mV
OUTPUT VOLTAGE SWING	V_O	$R_L \geq$ 2 kΩ $R_L \geq$ 600 Ω	±12.0 ±10.0	±13.8 ±11.5		±11.5 ±10.0	±13.5 ±11.5		V V
SLEW RATE	SR	$R_L \geq$ 2 kΩ[4]	1.7	2.8		1.7	2.8		V/µs
GAIN BANDWIDTH PROD.	GBW	Note 4	5	8		5	8		MHz
OPEN-LOOP OUTPUT RESISTANCE	R_O	V_O = 0, I_O = 0		70			70		Ω
POWER CONSUMPTION	P_d	Each Amplifier		90	140		100	170	mW
OFFSET ADJUSTMENT RANGE		R_p = 10 kΩ		±4			±4		mV

NOTES

[1]Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. E Grade specifications are guaranteed fully warmed up.

[2]Long term input offset voltage stability refers to the average trend line of V_{OS} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 µV. Refer to the Typical Performance Curve.

[3]Sample tested.

[4]Parameter is guaranteed by design.

[5]See test circuit and frequency response curve for 0.1 Hz to 10 Hz tester.

[6]See test circuit for current noise measurement.

[7]Guaranteed by input bias current.

Specifications subject to change without notice.

SPECIFICATIONS

Individual Amplifier Characteristics (V_S = ±15 V, –25°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP227E Min	OP227E Typ	OP227E Max	OP227G Min	OP227G Typ	OP227G Max	Unit
INPUT OFFSET VOLTAGE	V_{OS}	Note 1		40	140		85	280	μV
AVERAGE INPUT OFFSET DRIFT	TCV_{OS} TCV_{OSn}	Note 2		0.5	1.0		0.5	1.8	μV/°C
INPUT OFFSET CURRENT	I_{OS}			10	50		20	135	nA
INPUT BIAS CURRENT	I_B			±14	±60		±25	±150	nA
INPUT VOLTAGE RANGE	IVR		±10	±11.8		±10	±11.8		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±10 V	110	124		96	118		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4.5 V to ±18 V		2	15		2	32	μV/V
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	750	1500		450	1000		V/mV
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±11.7	±13.6		±11.0	±13.3		V

Matching Characteristics (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP227E Min	OP227E Typ	OP227E Max	OP227G Min	OP227G Typ	OP227G Max	Unit
INPUT OFFSET VOLTAGE MATCH	ΔV_{OS}			25	80		55	300	μV
AVERAGE NONINVERTING CURRENT	I_B+	$I_B+ = \frac{I_B+_A + I_B+_B}{2}$		±10	±40		±15	±90	Bias nA
NONINVERTING OFFSET CURRENT	$I_{OS}+$	$I_{OS}+ = I_B+_A - I_{B+B}$		±12	±60		±20	±130	nA
INVERTING OFFSET CURRENT	$I_{OS}-$	$I_{OS}- = I_B-_A - I_B-_B$		±12	±60		±20	±130	nA
COMMON-MODE REJECTION RATIO MATCH	ΔCMRR	V_{CM} = ±11 V	110	123		97	117		dB
POWER SUPPLY REJECTION RATIO MATCH	ΔPSRR	V_S = ±4 V to ±18 V		2	10		2	20	μV/V
CHANNEL SEPARATION	CS	Note 1	126	154		126	154		dB

NOTES
[1]Input Offset Voltage measurements are performed by automated equipment approximately 0.5 seconds after application of power.
[2]The TCV_{OS} performance is within the specifications unnulled or when nulled with R_P = 8 kΩ to 20 kΩ, optimum performance is obtained with R_P = 8 kΩ.
[3]Sample tested.

Specifications subject to change without notice.

Matching Characteristics (V_S = ±15 V, T_A = -25°C to +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP227E Min	OP227E Typ	OP227E Max	OP227G Min	OP227G Typ	OP227G Max	Unit
INPUT OFFSET VOLTAGE MATCH	ΔV_{OS}			40	140		90	400	µV
INPUT OFFSET TRACKING	$TC\Delta V_{OS}$	Nulled or Unnulled*		0.3	1.0		0.5	1.8	µV/°C
AVERAGE NONINVERTING BIAS CURRENT	I_B+	$I_B+ = \frac{I_B+_A + I_B+_B}{2}$		±14	±60		±25	±170	nA
AVERAGE DRIFT OF NONINVERTING BIAS CURRENT	TCI_B+			80			180		pA/°C
NONINVERTING OFFSET CURRENT	$I_{OS}+$	$I_{OS}+ = I_B+_A - I_B+_B$		±20	±90		±35	±250	nA
AVERAGE DRIFT OF NONINVERTING OFFSET CURRENT	$TCI_{OS}+$			130			250		pA/°C
INVERTING OFFSET CURRENT	$I_{OS}-$	$I_{OS}- = I_B-_A - I_B-_B$		±20	±90		±35	±250	nA
COMMON-MODE REJECTION RATIO MATCH	ΔCMRR	V_{CM} = ±10 V	106	120		90	112		dB
POWER SUPPLY REJECTION RATIO MATCH	ΔPSRR	V_S = ±4.5 V to ±18 V		2	15		3	32	µV/V

NOTES
*Sample tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . ±22 V
Input Voltage[1] . . . . ±22 V
Output Short-Circuit Duration . . . . Indefinite
Differential Input Voltage[2] . . . . ±0.7 V
Differential Input Current[2] . . . . ±25 mA
Storage Temperature Range . . . . –65°C to +150°C
Operating Temperature Range
  OP227E, OP227G . . . . –25°C to +85°C
Lead Temperature (Soldering 60 sec) . . . . 300°C

NOTES
[1]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[2]The OP227 inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current should be limited to 25 mA.
[3]θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for CERDIP package.

THERMAL CHARACTERISTICS

Thermal Resistance

14-Lead CERDIP
  θ_{JA}[3] = 106°C/W
  θ_{JC} = 16°C/W

ORDERING GUIDE

T_A = 25°C V_{OS} MAX (μV)	Hermetic DIP 14-Lead	Operating Temperature Range
80	OP227EY	IND
180	OP227GY	IND

For military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp.

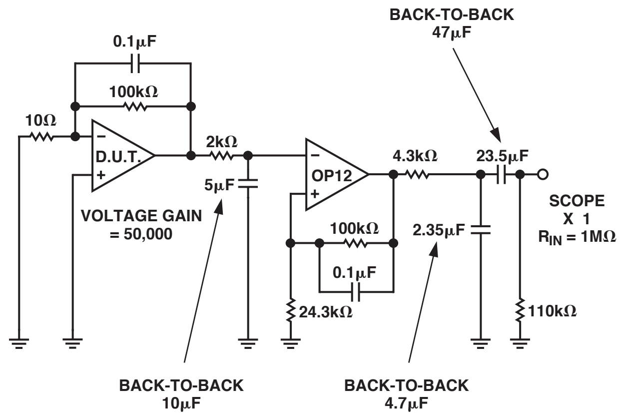
SMD Part Number	ADI Equivalent
5962-8688701CA*	OP227AYMDA

*Not recommended for new design, obsolete April 2002.

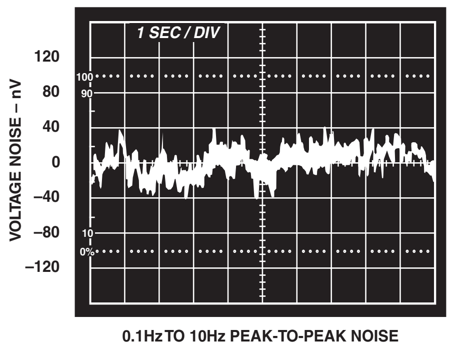
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP227 features propriety ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefor, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

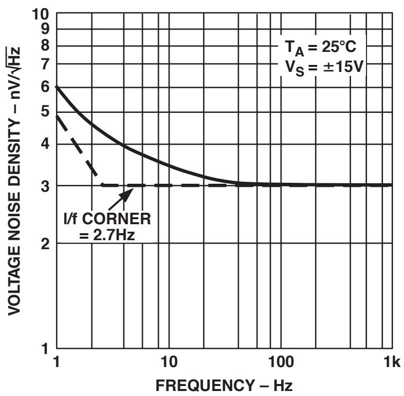
OP227–Typical Performance Characteristics



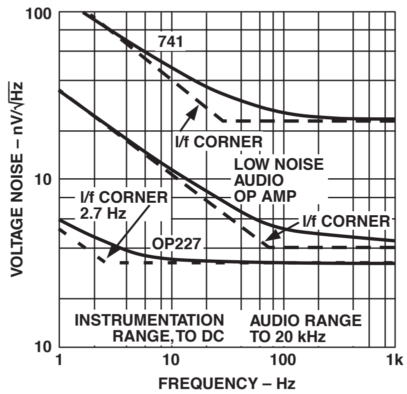
TPC 1. Voltage Noise Test Circuit (0.1 Hz to 10 Hz p-p)



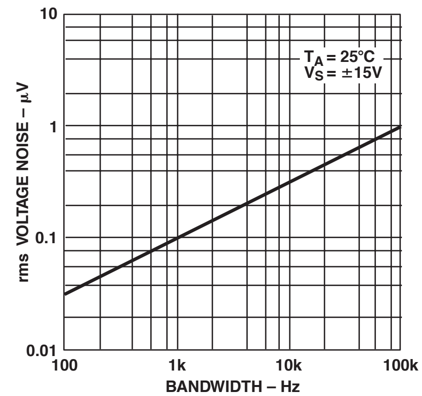
TPC 2. Low Frequency Noise (Observation Must Be Limited to 10 Seconds to Ensure 0.1 Hz Cutoff)



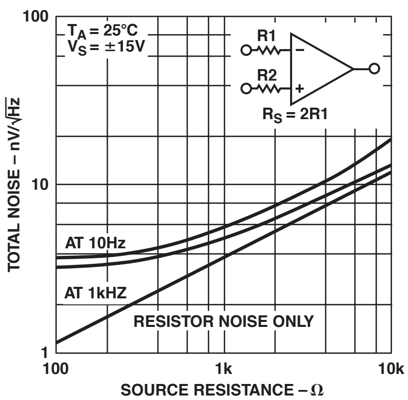
TPC 3. Voltage Noise Density vs. Frequency



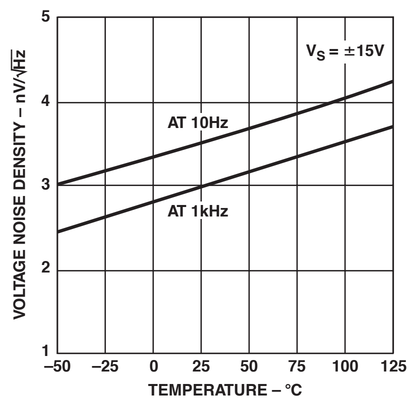
TPC 4. Comparison of Op Amp Voltage Noise Spectra



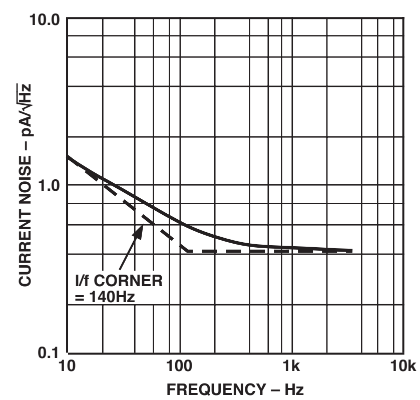
TPC 5. Input Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)



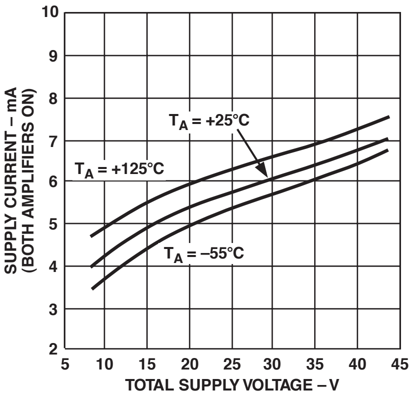
TPC 6. Total Noise vs. Source Resistance



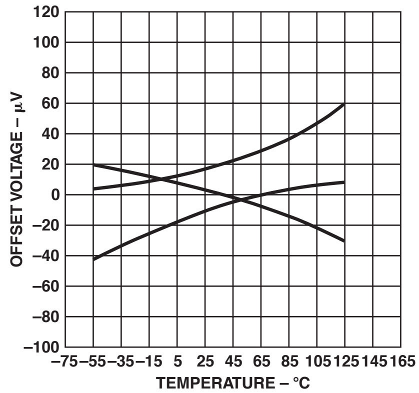
TPC 7. Voltage Noise Density vs. Temperature



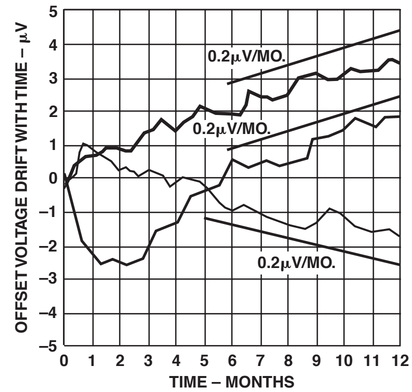
TPC 8. Current Noise Density vs. Frequency



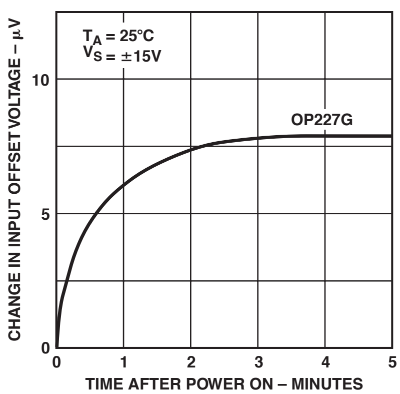
TPC 9. Supply Current vs. Supply Voltage



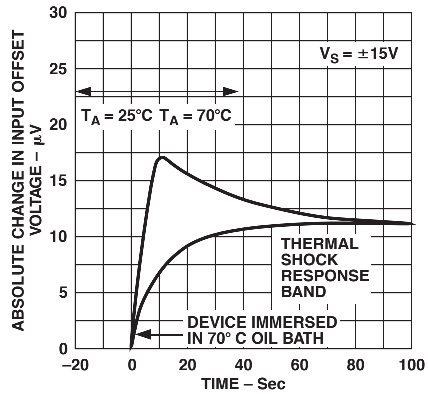
TPC 10. Offset Voltage Drift of Representative Units



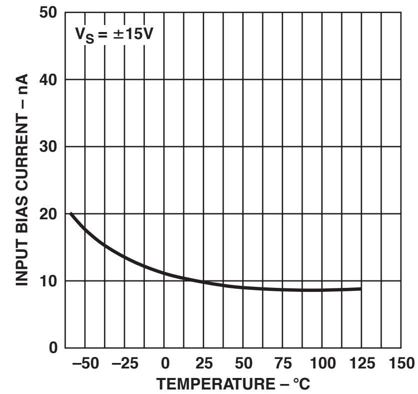
TPC 11. Offset Voltage Stability with Time



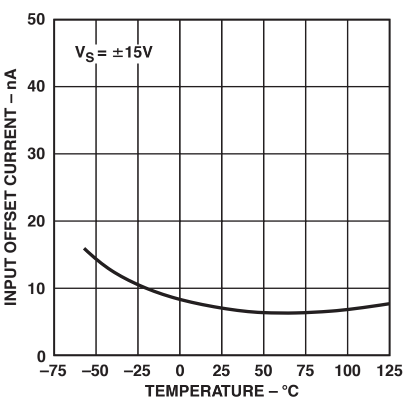
TPC 12. Warm-Up Drift



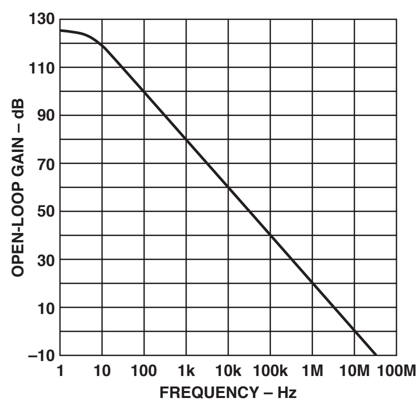
TPC 13. Offset Voltage Change Due to Thermal Shock



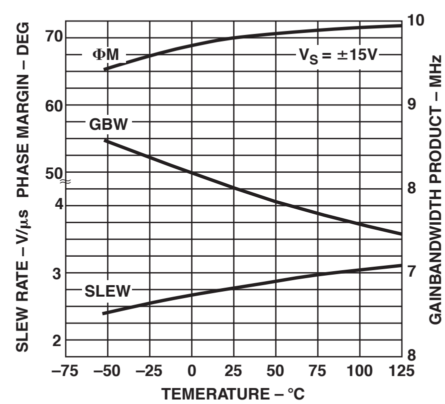
TPC 14. Input Bias Current vs. Temperature



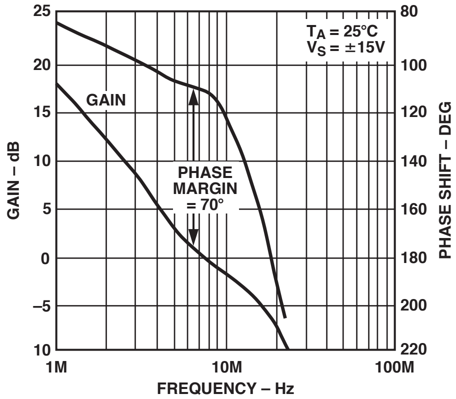
TPC 15. Input Offset Current vs. Temperature



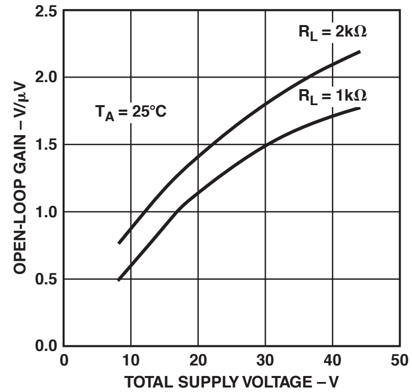
TPC 16. Open-Loop Gain vs. Frequency



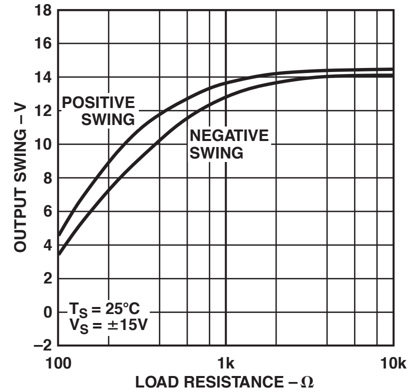
TPC 17. Slew Rate, Gain Bandwidth Product, Phase Margin vs. Temperature



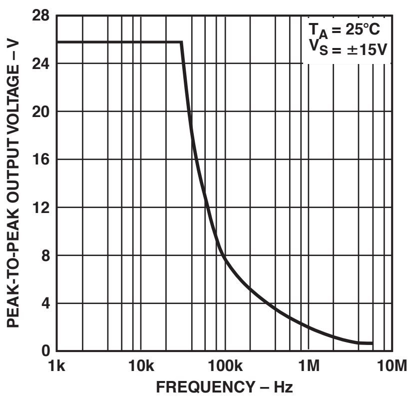
TPC 18. Gain, Phase Shift vs. Frequency



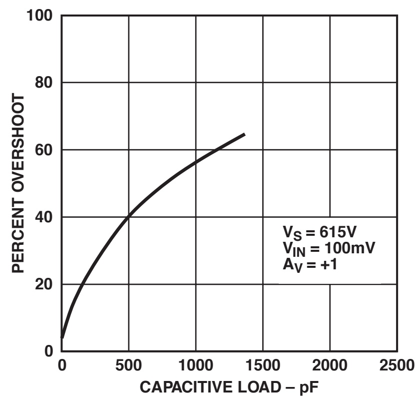
TPC 19. Open-Loop Gain vs. Supply Voltage



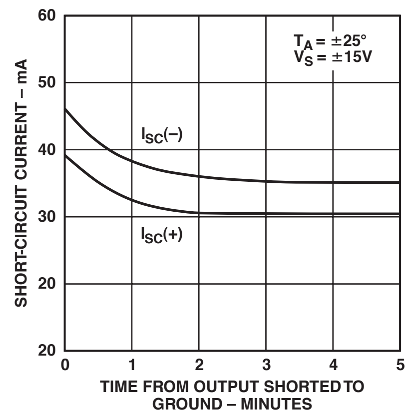
TPC 20. Output Swing vs. Resistive Load



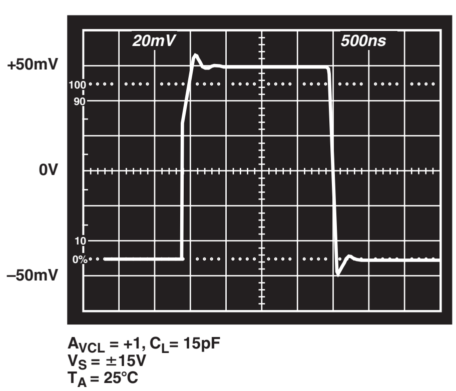
TPC 21. Maximum Undistorted Output vs. Frequency



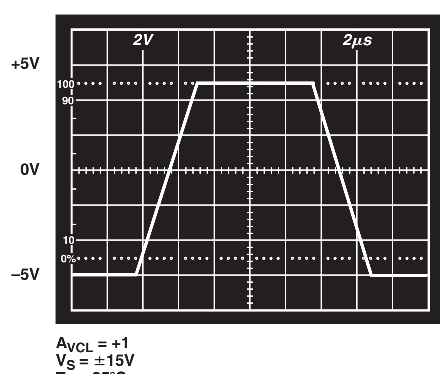
TPC 22. Small-Signal Overshoot vs. Capacitive Load



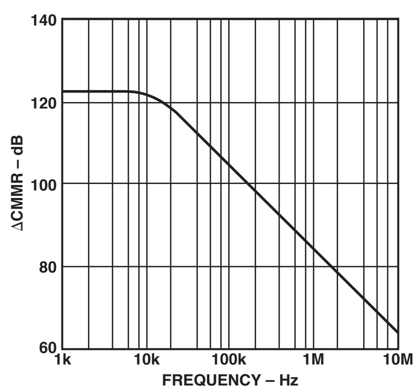
TPC 23. Short-Circuit Current vs. Time



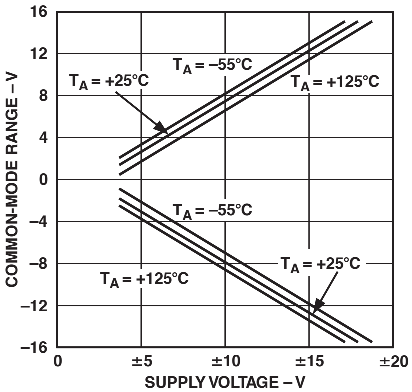
TPC 24. Small-Signal Transient Response



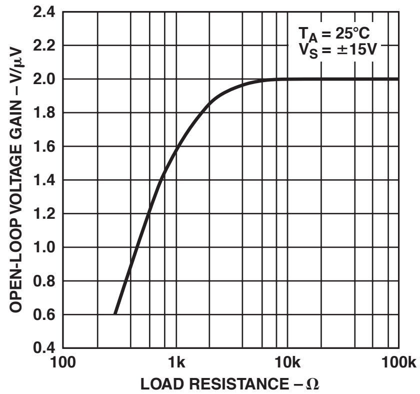
TPC 25. Large-Signal Transient Response



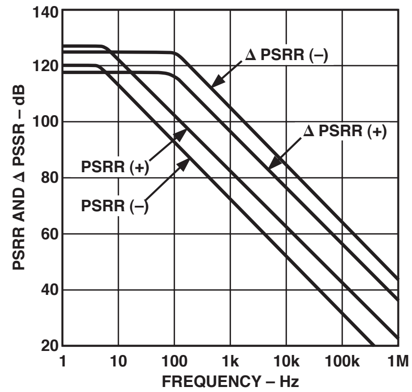
TPC 26. Matching Characteristic CMRR Match vs. Frequency



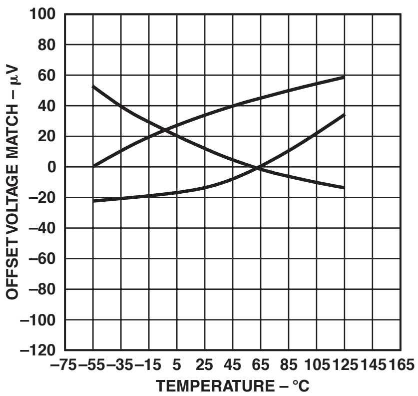
TPC 27. Common-Mode Input Range vs. Supply Voltage



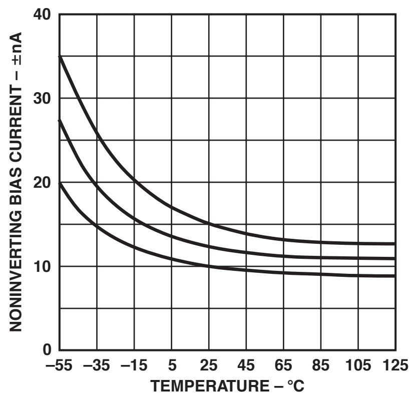
TPC 28. Open-Loop Voltage Gain vs. Load Resistance



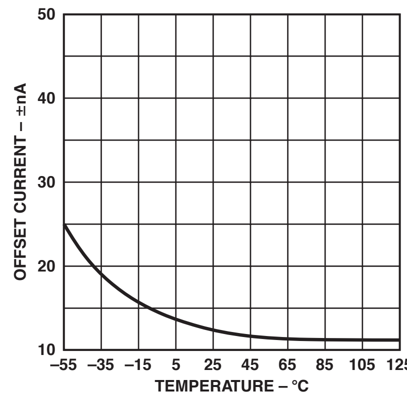
TPC 29. PSRR and ΔPSRR vs. Frequency



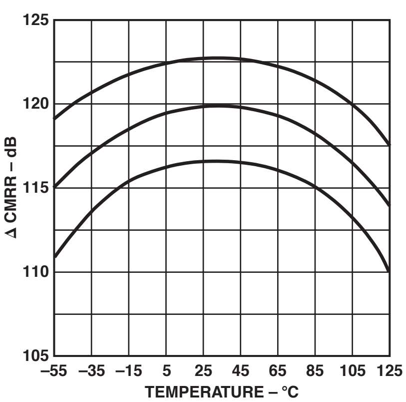
TPC 30. Matching Characteristic: Drift of Offset Voltage Match of Representative Units



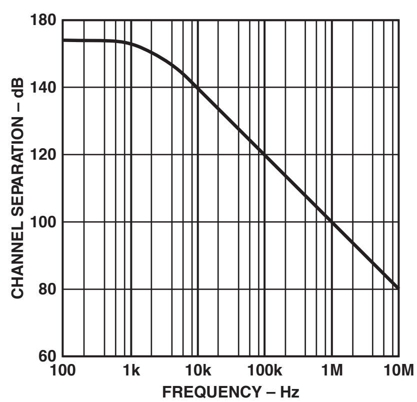
TPC 31. Matching Characteristic: Average Noninverting Bias Current vs. Temperature



TPC 32. Matching Characteristic: Average Offset Current vs. Temperature (Inverting or Noninverting)



TPC 33. Matching Characteristic: CMRR Match vs. Temperature



TPC 34. Channel Separation vs. Frequency

BASIC CONNECTIONS

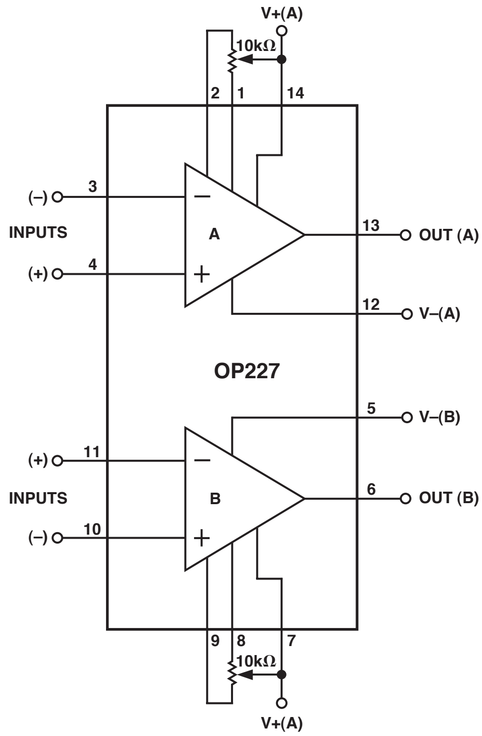


Figure 1. Offset Nulling Circuit

APPLICATIONS INFORMATION

Noise Measurements

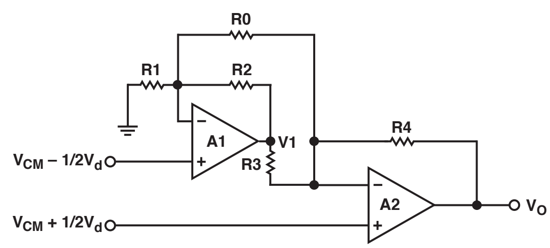
To measure the 80 nV peak-to-peak noise specification of the OP227 in the 0.1 Hz to 10 Hz range, the following precautions must be observed:

- The device must be warmed up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4 μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
- For similar reasons, the device must be well shielded from air currents. Shielding minimizes thermocouple effects.
- Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
- The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10-seconds. As shown in the noise-tester frequency-response curve, the 0.1 Hz corner is defined by only one zero to eliminate noise contributions from the frequency band below 0.1 Hz.
- A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage-density measurement will correlate well with a 0.1 Hz to 10 Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

Instrumentation Amplifier Applications of the OP227

The excellent input characteristics of the OP227 make it ideal for use in instrumentation amplifier configurations where low level differential signals are to be amplified. The low noise, low input offsets, low drift, and high gain, combined with excellent CMR provide the characteristics needed for high performance instrumentation amplifiers. In addition, CMR versus frequency is very good due to the wide gain bandwidth of these op amps.

The circuit of Figure 2 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two op amp instrumentation amplifier features independent adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to non-inverting op amp inputs.



$$V_O = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R0}\right]V_d + \frac{R4}{R3}\left(\frac{R3}{R4} - \frac{R2}{R1}\right)V_{CM}$$

Figure 2. Two Op Amp Instrumentation Amplifier Configuration

The output voltage V_O, assuming ideal op amps, is given in Figure 2. the input voltages are represented as a common-mode input, V_{CM}, plus a differential input, V_d. The ratio R3/R4 is made equal to the ratio R2/R1 to reject the common mode input V_{CM}. The differential signal V_O is then amplified according to:

$$V_O = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R_O}\right)V_d\text{, where } \frac{R3}{R4} = \frac{R2}{R1}$$

Note that gain can be independently varied by adjusting R_O. From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R1, R2, R3, and R4 approximately equal. Designing R1, R2, R3, and R4 as R_N allows the output equation to be further simplified:

$$V_O = 2\left(1 + \frac{R_N}{R_O}\right)V_d\text{, where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2. The output of A1 is:

$$V_1 = -\left(1+\frac{R_N}{R_O}\right)V_d + 2\,V_{CM}$$

If the instrumentation amplifier was designed for a gain of 10 and maximum V_d of ±1 V, then R_N/R_O would need to be four and V_O would be a maximum of ±10 V. Amplifier A1 would have a maximum output of ±5 V plus 2 V_{CM}, thus a limit of ±10 V on the output of A1 would imply a limit of ±2.5 V on V_{CM}. A nominal value of 10 kΩ for R_N is suitable for most applications. A range of 20 Ω to 2.5 kΩ for R_O will then provide a gain range of 10 to 1000. The current through R_O is V_d/R_O, so the amplifiers must supply ±10 mV/20 Ω (or ±0.5 mA) when the gain is at the maximum value of 1000 and V_d is at ±10 mV.

Rejecting common-mode inputs is important in accurately amplifying low level differential signals. Two factors determine the CMR in this instrumentation amplifier configuration (assuming infinite gain):

- CMR of the op amps
- Matching of the resistor network ratios (R3/R4 = R2/R1)

In this instrumentation amplifier configuration error due to CMR effect is directly proportional to the CMR match of the op amps. For the OP227, this DCMR is a minimum of 97 dB for the "G" and 110 dB for the "E" grades. A DCMR value of 100 dB and a common-mode input range of ±2.5 V indicates a peak input-referred error of only ±25 μV. Resistor matching is the other factor affecting CMR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R1, R2, R3, and R4 are approximately equal (R_N will be the nominal value), then CMR for this instrumentation amplifier configuration will be approximately A_d divided by $4\Delta R/R_N$. CMR at differential gain of 100 would be 88 dB with resistor matching of 0.01%. Trimming R1 to make the ratio R3/R4 equal to R2/R1 will raise the CMR until limited by linearity and resistor stability considerations.

The high open-loop gain of the OP227 is very important to achieving high accuracy in the two op amp instrumentation amplifier configuration. Gain error can be approximated by:

$$Gain\ Error \sim \frac{1}{1+\dfrac{A_d}{A_{O2}}}, \frac{A_d}{2A_{O1}A_{O1}} < 1$$

where A_d is the instrumentation amplifier differential gain and A_{O2} is the open loop gain of op amp A2. This analysis assumes equal values of R1, R2, R3, and R4. For example, consider an OP227 with A_{O2} of 700 V/mV. Id the differential gain A_d were set to 700, then the gain error would be 1/1.001, which is approximately 0.1%.

Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{O1} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect would be approximately:

$$CME \sim \frac{2A_d}{1+\dfrac{A_d}{A_{O2}}}, \frac{1}{A_{O1}} V_{CM}$$

For $A_d/A_{01} < 1$, this simplifies to $(2A_d/A_{01})\ 3\ V_{CM}$. If the op amp gain is 700 V/mV, V_{CM} is 2.5 V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5 mV.

A compete instrumentation amplifier designed for a gain of 100 is shown in Figure 3. It has provision for trimming of input offset voltage, CMR, and gain. Performance is excellent due to the high gain, high CMR, and low noise of the individual amplifiers combined with the tight matching characteristics of the OP227 dual.

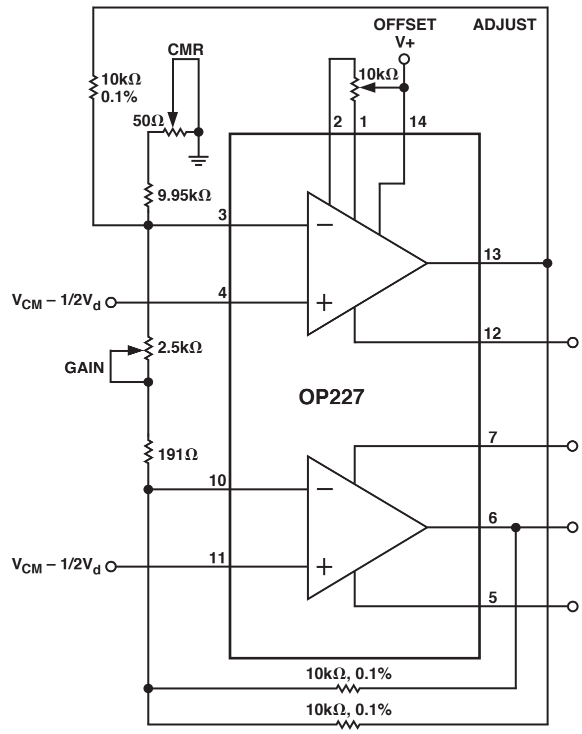


Figure 3. Two Op Amp Instrumentation Amplifier Using OP227 Dual

A three op amp instrumentation amplifier configuration using the OP227 and OP27 is recommended for applications requiring high accuracy over a wide gain range. This circuit provides excellent CMR over a wide frequency range. As with the two op amp instrumentation amplifier circuits, the tight matching of the two op amps within the OP227 package provides a real boost in performance. Also, the low noise, low offset, and high gain of the individual op amps minimize errors.

A simplified schematic is shown in Figure 4. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM}. The output stage then rejects the common-mode input. With ideal op amps and no resistor matching errors, the outputs of each amplifier will be:

$$V_1 = -\left(1+\frac{2R1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_2 = -\left(1+\frac{2R1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_O = V_2 - V_1 = \left(1+\frac{2R1}{R_O}\right)V_d$$

$$V_O = A_d\,V_d$$

The differential gain A_d is 1 + 2R1/R0 and the common-mode input V_{CM} is rejected.

While output error due to input offsets and noise are easily determined, the effects of finite gain and common-mode rejection are more subtle. CMR of the complete instrumentation amplifier is directly proportioned to the match in CMR of the input op amps. This match varies from 97 dB to 110 dB minimum for the OP227. Using 100 dB, then the output response to a common-mode input V_{CM} would be:

$$\left[V_O\right]_{CM} = A_d\, V_{CM} \times 10^{-5}$$

CMRR of the instrumentation amplifier, which is defined as 20 log10A_d/A_{CM}, is simply equal to the ΔCMRR of the OP227. While this ΔCMRR is already high, overall CMRR of the complete amplifier can be raised by trimming the output stage resistor network.

Finite gain of the input op amps causes a scale factor error and a small degradation in CMR. Designating the open-loop gain of op amp A_1 as A_{O1}, and op amp A_2 as A_{O2}, then the following equation approximates output:

$$V_O \sim \frac{1}{1+\frac{R1}{R0}\left(\frac{1}{A_{O1}}+\frac{1}{A_{O2}}\right)}\left(A_d\, V_d + \frac{2R1}{R0}\left(\frac{1}{A_{O1}}-\frac{1}{A_{O2}}\right)V_{CM}\right)$$

This can be simplified by defining A_O as the nominal open-loop gain and ΔA0 as the differential open-loop gain. Then:

$$V_O \sim \frac{1}{1+\frac{R1}{R0}\frac{1}{A_O}}\left(A_d\, V_d + \frac{2R1}{R0}\frac{\Delta A_O}{A_O^{\;2}}\, V_{CM}\right)$$

The high open-loop gain of each amplifier within the OP227 (700,000 minimum at 25°C in $R_L \geq 2$ kΩ) assures good gain accuracy even at high values of A_d. The effect of finite open-loop gain on CMR can be approximated by:

$$CMRR \sim \frac{A_O^{\;2}}{\Delta A_O}$$

If $\Delta A_O/A_O$ were 6% and A_O were 600,000, then the CMRR due to finite gain of the input op amps would be approximately 140 dB.

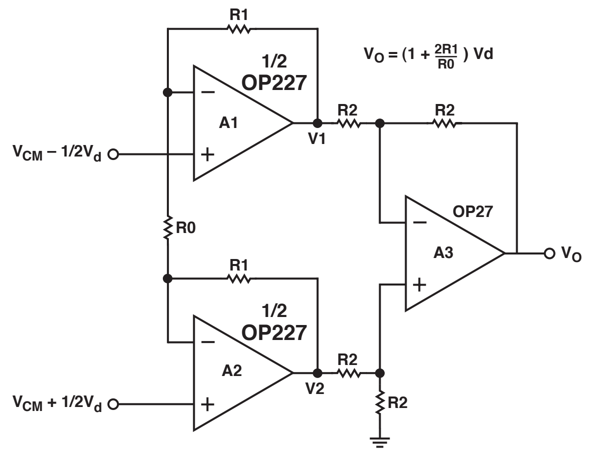


Figure 4. Three Op Amp Instrumentation Amplifier Using OP227 and OP27

The unity-gain output stage contributes negligible error to the overall amplifier. However, matching of the four resistor R2 network is critical to achieving high CMR. Consider a worst-case situation where each R2 resistor had an error of ±**Δ**R2. If the resistor ratio is high on one side and low on the other, then the common-mode gain will be 2**Δ**R2/2**Δ**R2. Since the output stage gain is unity, CMRR will then be R2/2**Δ**R2. It is common practice to maximize overall CMRR for the total instrumentation amplifier circuit.

High Speed Precision Rectifier

The low offsets and excellent load driving capability of the OP27 are key advantages in this precision rectifier circuit. The summing impedances can be as low as 1 kΩ which helps to reduce the effects of stray capacitance.

For positive inputs, D2 conducts and D1 is biased OFF. Amplifiers A1 and A2 act as a follower with output-to-output feedback and the R1 resistors are not critical. For negative inputs, D1 conducts and D2 is biased OFF. A1 acts as a follower and A2 serves as a precision inverter. In this mode, matching of the two R1 resistors is critical to gain accuracy.

Typical component values are 30 pF for C1 and 2 kΩ for R3. The drop across D1 must be less than the drop across the FET diode D2. A 1N914 for D1 and a 2N4393 for the JFET were used successfully.

The circuit provides full-wave rectification for inputs of up to ±10 V and up to 20 kHz in frequency. To assure frequency stability, be sure to decouple the power supply inputs and minimize any capactive loading. An OP227, which is two OP27 amplifiers in a single package, can be used to improve packaging density.

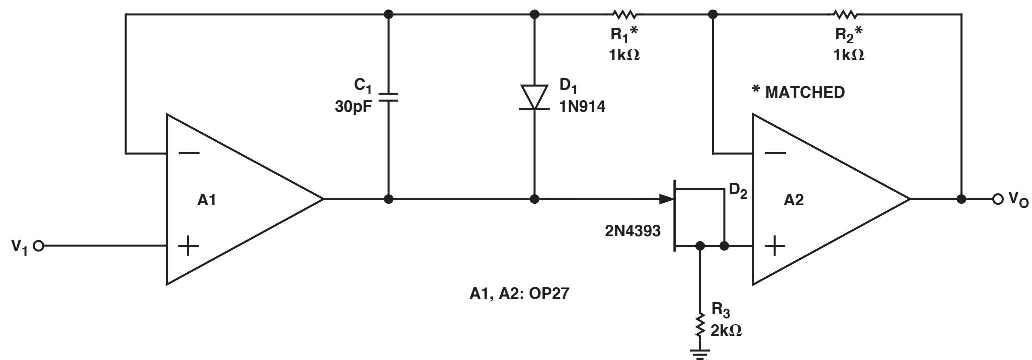
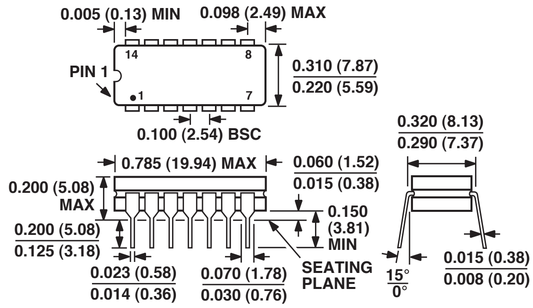


Figure 5. High Speed Precision Rectifier

OUTLINE DIMENSIONS

14-Lead Ceramic Dip – Glass Hermetic Seal [CERDIP] (Q-14)

Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location **Page**

10/02—Data Sheet changed from REV. 0 to REV. A.

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